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Energy Efficient CRC Design for Processor of Workstation, and Server using LVCMOS

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Abstract

In our work we have designed CRC using the LVCMOS IO standards which are stands for Low Voltage Complementary Metal Oxide Semiconductor. In this work we have worked with four kinds of LVCMOS (LVCMOS 12, LVCMOS 15, LVCMOS 18, LVCMOS 25). For LVCMOS 12 when we scaled down the frequency form 50GHz to 10 GHz we found 64.41% reduction in total power. For LVCMOS 15 when we change down the frequency form 50GHz to 10GHz we found 67.58% reduction in total power. For LVCMOS 18 when we scaled down the frequency form 50GHz to 10 GHz we found 69.54% reduction in total power. In last when we reduced the frequency form 50GHz to 10GHz in LVCMOS 25 we found 64.41% reduction in total power. Our CRC design is implemented on Virtex-6 FPGA family.

Keywords: 40 nm FPGA, CRC, Energy Efficient, Low Power, LVCMOS IO Standard

1. Introduction

In networking when we send data form one system to another system then we always try to ensure that receiver always get error free data. For that we can apply error detection techniques.

CRC is an error detection technique which is stands for Cyclic Redundancy Check, through CRC we can detect the error but we cannot resolve or correct the data.

In these techniques we append some check bits also called checksum to the message and send it to the receiver. After receiving the data receiver verified the checksum with data and assert that error would occur or not. If there is an error then receiver sends Negative Acknowledgment (NCK) to sender for retransmission of the packets.

In our paper we have design 8 bit CRC Polynomial which is also called CRC-8-CCITT. Equation (1) shows our CRC polynomial equation and figure 1 shows the circuit diagram generated by our polynomial.

$$P(x) = x^8 + x^2 + x^1 + x^0 \quad (1)$$

Figure 1. Circuit diagram of CRC polynomial.

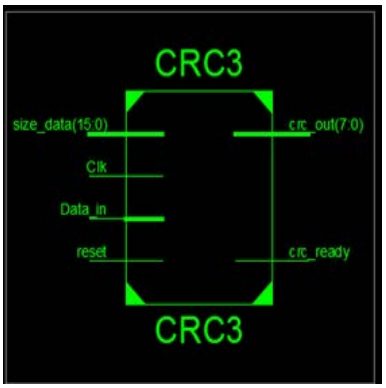

Figure 2. Top Level of schematic of CRC.

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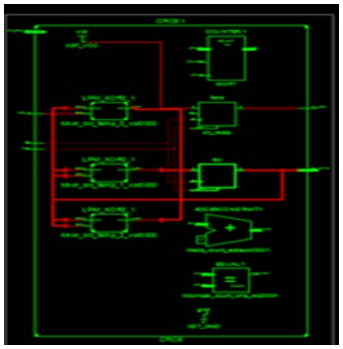

Figure 3. RTL schematic of CRC.

In Figure 3 and Figure 4 we have shown the Top Level of Schematic of CRC and RTL Schematic of CRC.

2. Related Work

There is 67.04% dynamic power reduction with LVCMOS12[2]. There is 85.18% power reduction when we migrate from LVCMOS33 based ALU design to LVCMOS12 based ALU design[3]. 28nm technology based FPGA deliver energy efficient design[3,4]. LVCMOS is not only used in energy efficient design of ALU[2,3] but also in energy efficient Sindhi unicode reader[4], thermal aware energy efficient Vedic multiplier[5], power optimization of pseudo noise based optical transmitter[6], energy efficient solar charge sensor[7] and energy efficient energy efficient Frequency Meter[8].

3. Results

We have opted VHDL language to design CRC and implemented it on Virtex-6 family.

Table 1. Power consumption at LVCMOS12

	Clock	Logic	Signals	IOs	Leakage	Total Power
10 GHz	0.349	0.007	0.030	0.668	1.315	2.370
20 GHz	0.698	0.010	0.058	1.336	1.340	3.442
30 GHz	1.047	0.012	0.086	2.005	1.365	4.514
40 GHz	1.395	0.014	0.113	2.673	1.392	5.587
50 GHz	1.744	0.015	0.140	3.341	1.420	6.661

In the Table 1 we have worked with LVCMOS12. In this table we found that when we migrate from 50GHz to 10 GHz then we reduce the power consumption by 64.41%.We have also converted this data through bar graph as shown in Figure 4.

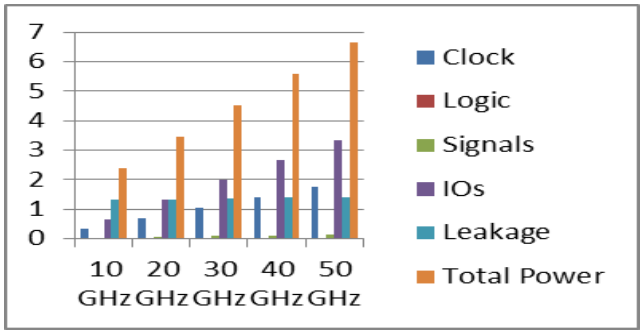

Figure 4. Power analysis at LVCMOS 12.

Table 2. Power consumption at LVCMOS15

	Clock	Logic	Signals	IOs	Leakage	Total Power
10 GHz	0.349	0.007	0.030	0.998	1.323	2.708
20 GHz	0.698	0.010	0.058	1.996	1.356	4.118
30 GHz	1.047	0.012	0.086	2.993	1.391	5.528
40 GHz	1.395	0.014	0.113	3.991	1.427	6.941
50 GHz	1.744	0.015	0.140	4.989	1.466	8.355

In the Table 2 we have worked with LVCMOS15. In this table we found that when we migrate from 50GHz to 10 GHz then we reduce the power consumption by 67.58%. We have also converted this data through bar graph as shown in Figure 5.

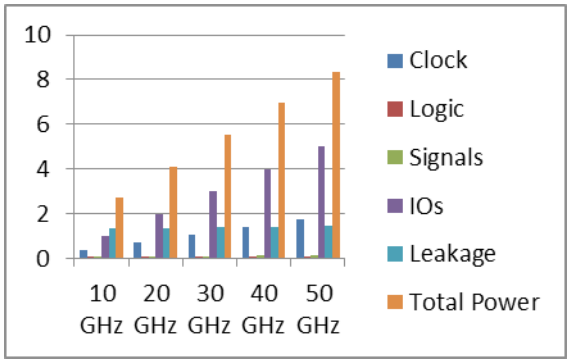

Figure 5. Power analysis at LVCMOS 15.

Table 3. Power consumption at LVCMOS 18

	Clock	Logic	Signals	IOs	Leakage	Total Power
10 GHz	0.349	0.007	0.030	2.088	1.298	3.015
20 GHz	0.698	0.010	0.058	2.596	1.371	4.733
30 GHz	1.047	0.012	0.086	3.893	1.415	6.452
40 GHz	1.395	0.014	0.113	5.191	1.461	8.174
50 GHz	1.744	0.015	0.140	6.489	1.510	9.900

In the Table 3 we have worked with LVCMOS18. In this table we found that when we migrate from 50GHz to10GHz then we reduce the power consumption by 69.54%. We have also converted this data through bar graph as shown in Figure 6

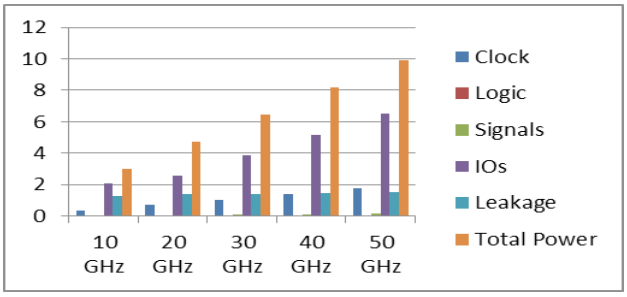

Figure 6. Power analysis at 3GHz.

Table 4. Power consumption at LVCMOS 25

	Clock	Logic	Signals	IOs	Leakage	Total Power
10 GHz	0.349	0.007	0.030	2.088	1.350	3.825
20 GHz	0.698	0.010	0.058	4.177	1.413	6.356
30 GHz	1.047	0.012	0.086	6.265	1.482	8.891
40 GHz	1.395	0.014	0.113	8.354	1.558	11.433
50 GHz	1.744	0.015	0.140	10.442	1.605	13.947

In the Table 4 we have worked with LVCMOS12. In this table we found that when we migrate from 50GHz to 10 GHz then we reduce the power consumption by 72.57%. We have also converted this data through bar graph as shown in Figure 7.

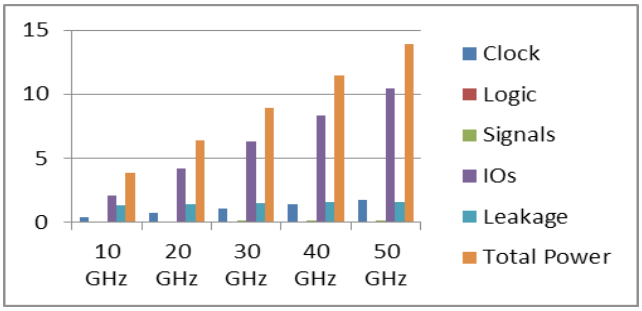

Figure 7. Power analysis at 3GHz.

4. Conclusion

In our work we have calculated total power consumption using different-different family of LVCMOS (LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25) at different-different frequency. We found that LVCMOS 12 is most energy efficient IO standard compare to other LVCMOS IO standard. We also found that there is no change in Logic, Signal and IOs.

5. Future Scope

In this work, CRC Design is implemented on Virtex-6, but we have a scope to redesign this CRC on latest 65nm Virtex-5 and 40nm Virtex-6, 90nm Virtex-4 FPGA to make the most energy efficient CRC for data transmission. Instead of LVCMOS IO standards we can use other IO standards like SSTL and LVDCI.

6. Acknowledgment

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